

MODIS Team Meeting Minutes

Minutes of the MODIS Team Meeting held on Tuesday July 18, 1995.

Action Items:

94. Provide a detailed (high fidelity) analysis of scatter in the scan cavity. The results would determine the need for PF near field scatter measurements vs scan angle. Assigned to Guenther 8/23/94 Preliminary results due 10/15/94. Final due 2/28/95. New due date 4/28/95
112. Analyze the ScMA optical design. Assigned to Waluschka 1/31/95. Due 2/ 7/95

Distribution:

Richard Weber	Bruce Guenther	Larissa Graziani
John Bauernschub	George Daelemans	Bob Martineau
Rosemary Vail	Mitch Davis	Bob Silva
Lisa Shears	Ken Anderson	Robert Kiwak
Mike Roberto	Rick Sabatino	Harvey Safren
Gene Waluschka	Cherie Congedo	Ed Knight
Bill Barnes	Jose Florez	Harry Montgomery
Les Thompson	Gerry Godden	Marvin Maxwell
John Bolton	Sal Cicchelli	Bill Mocarsky
Pat Delosa		

The following items were distributed:

- 1) Weekly Status Report #198
- 2) SBRC Memos submission from week #1909
- 3) Minutes of the previous team meeting

MODIS Technical Weekly July 21, 1995 sent to MODIS.Review 7/24/95 at about 5 PM

1.0 Summary

The good news is that closing GSFC is not in the FY-96 spending bill put forward by the House Appropriations Committee. There is still the matter of the funding level for Goddard to be worked out over the next several weeks.

A MODIS Characterization Support Team Science Team Review was held on July 18. A preliminary overview of a preliminary report from Breault Research Organization entitled "Stray Radiation Analysis of the MODIS System" was presented by G. Godden. Presentations were also made by B. Guenther, M. Hopkins, E. Knight, and J. Barker. BRO analyzed near field scatter for the aft optics for the PFM. Data which directly relates predicted performance to the MODIS specification was not presented in the initial report and will be provided by BRO.

Bob Martineau announced the VIS, NIR, and SWIR FPAs have been delivered. The LWIR detector assembly is awaiting a reworked filter/bezel assembly and is expected to be delivered to the systems division on July 28.

Jose Florez reported that the test ACE/ACE and ACE/Clock/Bias cards have completed individual bench level check-out; the MEM backplane connectors were being installed the week of July 21; and the source of MEM FBAD problem has been identified as a design flaw in one of the ACTELs in the Formatter. Jose includes a memo from SBRC which describes the FBAD problem and concludes this problem can be fixed in software.

2.0 MODIS Characterization Support Team Science Team Review

This includes a brief summary of four important topics from the review. Concerns have been raised with regard to expected PFM performance. SBRC is identifying what is planned for the PFM in response to any MODIS specification which was not met on the EM.

a) Breault Analysis for Stray Light

This preliminary report was received on July 19 by MODIS project personnel and has been sent to SBRC for review and comment. The report is also being reviewed by GSFC MODIS science, engineering, and management personnel. BRO will update the report to directly display response from a cloud on the focal plane as a function of distance from the cloud for a few representative bands. This can be related directly to the MODIS transient response specification.

b) Engineering Model Test Results

These results include scatter, ghosting, and crosstalk. The EM optics had smudges. EM dichroic 1 had very high scatter. Care is needed in using EM transient response performance as a starting point toward predicting PFM performance.

c) Image Restoration

Image restoration will be considered. However, Gerry Godden and Al McKay included a topic on key issues related to image cloud edge radiometry restoration. These included image cloud edge restoration being typically limited to minor improvements of probably of the order of a few percent, with probably low or corrected crosstalk, and probably over small scan angles. Also, gain changes would be needed for several bands, which would affect SNR.

d) TAC

One concern about the Test Analysis Computer (TAC) software was that SBRC was behind in completing the TAC software and delivery of the source code was delayed. The source code for the TAC software in pre-release electronic form is in process of being sent to GSFC.

Finally, there is the question of expected PFM performance. There are several changes planned for the PFM which should improve performance relative to the EM. Ghosting fixes will substantially reduce ghosting for the PFM. The new dichroic 1 has much lower scatter. Stripes are being painted on the PFM focal plane to reduce crosstalk. It remains to be seen if any additional changes will be necessary in the aft optics.

3.0 Bob Martineau

(VIS, NIR, SWIR FPAs delivered; LWIR detector assembly awaiting a reworked filter/bezel assembly)

email from Bob Martineau 7/21/95 11:09 AM

- 1) PFM FPAs: VIS, NIR, SMWIR FPAs are delivered. The LWIR detector assembly is awaiting a reworked filter/bezel assembly which is now completing thermal cycle and vibration tests. The LWIR FPA is expected to be delivered to the systems division on July 28th.
- 2) FM1: The NIR detector assembly is in crosstalk testing. The VIS, SMWIR, and LWIR SCAs are being mounted on pedestal cable assemblies. A backup SCA is available for each of these FPAs.
- 3) FM2: VIS and NIR SCAs have been delivered to packaging for assembly. One acceptable SMWIR SCA has been identified. Four more are in hybridization and will be tested in August. The best of these 5 will be used for FM2.

Four LWIR SCAs have been tested and have one bad pixel each. Three more will be baked and tested. The best of these will be chosen for FM2. SBRC is looking for an LWIR SCA that has no bad pixels.

4.0 Jose Florez

(test ACE/ACE and ACE/Clock/Bias cards have completed individual bench level check-out; MEM backplane connectors being installed week of July 21; source of MEM FBAD problem identified as a design flaw in one of the ACTELs in the Formatter)

email from Jose 7/21/95 1:33 PM

Telecon with Ed Clement, 7/17/95, 4:30 PM

The test ACE/ACE and ACE/Clock/Bias cards have completed individual bench level check-out. Performance is better than the EM cards at the bench level. Quantitative results have to await testing at the instrument level, after the MEM is re-assembled following troubleshooting of the FBAD and FIFO non-empty swap problems.

The MEM backplane connectors are being installed this week. As soon as they are in place a fit check with the cards will be performed to verify alignment, and to test the insertion force required for mating. Wire-wrapping of the backplane is scheduled to start this Friday. GSFC is requesting from SBRC data for the card stackup analysis, and the card to backplane alignment and installation procedure to ascertain no stress is induced on the boards/connectors/pins.

The source of the MEM FBAD problem has been identified as a design flaw in one of the ACTELs in the Formatter. The problem can be circumvented with a software fix, and does not require modifications to the hardware. A memo describing the problem and proposed solution is appended below.

Jose reporting this week.

Memo from D. Selby, 20 July 95, W05147, EM Test Review Action Item 83 - BAD

This memo addresses Action Item 83 of the MODIS Engineering Model Test Review. This item covers the so-called FBAD problem in the Formatter section of the Main Electronics Module (MEM). FBAD is the hexadecimal code that is mistakenly used four times per scan as an FDDI interpacket gap control word.

This action item directs that the source of this error be determined, and if required, corrected.

The Format Engine includes a ping-pong packet header FIFO consisting of two identical FIFO memories and an FPGA-based controller. Each FIFO consists of a first-in-first-out memory and an output register. The FPGA controls accesses to each of the FIFOs by allocating one FIFO to the Single Board Computer (SBC) and the other to the Format Engine Writable Control Store (WCS) at any one time.

The WCS transfers header information from the packet header FIFO to the MM03 CCAs (the main science data FIFOs) in a two step process. The first step is to read the header word from the first-in-first-out memory and latch it into the output register. The second step is to enable the contents of the output register onto the Format Engine data bus and drive it across the backplane.

The FIFOs are automatically ping-ponged (re-directed) when the WCS reaches the end of the header information. A control bit in the last two header words controls this process by signaling the FPGA to swap FIFOs after the last word has been processed.

A mistake in the design of the FPGA controller, however, swaps FIFOs in-between the last read from the first-in-first-out memory and the subsequent enabling of the output register onto the data bus. This results in the wrong packet header FIFOs output being enabled onto the Format Engine data bus. Thus the last word of the previous set of headers is transferred (FBAD from the first set of dummy headers) instead of the last word of the current set of headers. The last word of the current set of headers therefore will be sent as the last word for the next set of FIFO headers, and so on.

Dummy headers are loaded at the start of each of the five mirror sectors. Dummy headers are headers to be consumed by the Format Engine while its input is enabled and its output is disabled. Consequently, the data values of the dummy headers are supposed to be meaningless, as they should never be output. The 12-bit value chosen for the data field in the dummy headers (including the interpacket gap word) was the value FBAD (hex). This value was chosen as a marker value to identify exactly the sort of error that has occurred.

This error occurs each time the packet header FIFOs are ping-ponged. The reason that it only creates a problem four times per scan is that the headers are stored in packet header FIFOs in the same addresses in each pass through the FIFO. In particular, the interpacket gap words are always stored in the same addresses in memory. Thus, the error will occur only on the interpacket gap word sent just before the each swap of actual header data. There are 60 headers loaded into each packet header FIFO before swapping. Since the SRCA requires at most 20 headers (10 frames of data times two headers per frame for day mode) all needed headers can be provided without swapping. The other four sectors all require at least one swap, which allows this error to occur, for a total of four FBAD errors per scan.

The simplest solution to this problem is to add code to the software which loads the dummy headers to replace the default value of FBAD in the last two words of the last dummy header with the correct interpacket gap for the current sector. This will ensure that the proper interpacket gap is in the output register of both halves of the packet header FIFO when the first load of real headers is consumed.

This interpacket gap problem does not invalidate the testing which has

been performed to date as the value FBAD is an acceptable interpacket gap value. (That is why testing was permitted to continue with this known problem.) The current range for interpacket gaps is F370 to FCD8).

It would be very difficult to correct this hardware error at this time.

Since we now know the source of the error, and also know that it will not cause other problems, we propose to handle it with the above described software fix.

end of D. Selby's memo.

Mike Roberto

July 21, 1995